Performance Evaluation of MAC schemes for wireless ATM systems with centralised control considering processing delays*

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Abstract - **This paper proposes a medium access control scheme for wireless ATM systems with centralised control, which considers the delays caused by the processing effort in the physical layer as well as in the data link control layer itself. These delays lead to reduced Quality of Service in terms of cell delay and cell delay variation. The approach presented is especially suited for utilisation in time division duplex systems to reduce the influence of processing delays as much as possible. Furthermore, the MAC protocol can be adapted to asymmetric traffic loads e.g. produced by distribution services like Video on Demand by using a flexible positioning strategy for the signalling bursts. Finally, by simulations the performance of the new MAC scheme is compared to the well known DSA++ (Dynamic Slot Assignment) protocol [1,2].**

I. INTRODUCTION

Asynchronous Transfer Mode (ATM) networks are becoming more and more important for modern multimedia applications. ATM allows to transfer various data of different services via the same network. Up to now ATM is only used in fixed networks, but during the last few years several investigations have been carried out to expand ATM networks to be accessed via wireless terminals (WT) in a cellular environment. Meanwhile, many projects have been launched with the objective to implement prototype systems, one of which is the German *ATMmobil* project, that is founded by the Federal Ministry of Education, Science, Research and Technology.

In cellular wireless networks one radio cell consists of several WTs and one central base station (BS). In general, the BS as the central instance controls the access to the shared medium and assigns transmission capacity to the WTs and to itself. To meet the requirements of statistical traffic loads in ATM networks, a dynamic capacity allocation scheme turned out to be more appropriate than static schemes [3,7]. Dynamic capacity assignments for a specific time interval (fixed or variable frame) are usually grouped in a signalling burst and broadcast by the BS to the WTs over the downlink for each frame. Based on this signalling concept many medium access control (MAC) schemes for wireless ATM (W-ATM) systems have been presented so far without taking into account realistic delays caused by the processing effort in the physical layer as well as in the data link control (DLC) layer itself of both sides, transmitter and receiver [1,5,6,7]. These delays lead to reduced Quality of Service (QoS) caused by decreased dynamic properties of the protocol in terms of cell delay and cell delay variation (CDV).

This paper introduces an enhanced MAC scheme with centralised control considering these processing delays. In section II the signalling scheme of the DSA++ protocol for a time division duplexing (TDD) system is presented. Section III gives an overview of delays within a W-ATM system and their effect on the dynamic properties of the MAC protocol is given. Section IV introduces an enhanced signalling scheme based on the DSA++ protocol. Finally, a performance evaluation based on simulations is presented in section V.

II. BASIC SIGNALLING SCHEME - DSA++

In this section a brief overview of the DSA++ protocol is given, only emphasising those items which are important for further understanding. Detailed descriptions can be found in [1,2].

Figure 1 shows the basic principle of the DSA++ scheme for a TDD system. The BS assigns each WT a certain transmission capacity in terms of time slots for a specific time interval, called signalling period (SP), depending on the requests of the WTs. Each time slot

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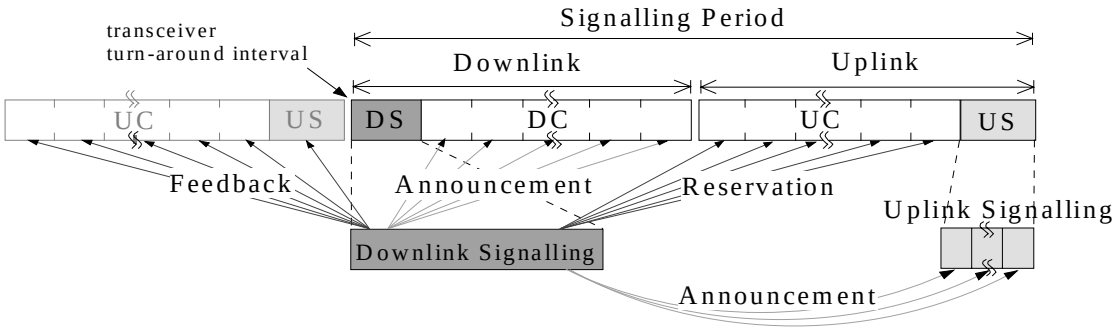

Figure 1: Basic signalling scheme - DSA ++

contains a data burst of one ATM cell including all necessary overhead for DLC protocol, training sequence, synchronisation, forward error correction (FEC) and guard time. The total amount of slots of a SP is variable and varies over time [3]. Each SP has one uplink and one downlink phase separated by a transceiver turn-around interval (TTI).

The uplink phase consists of a series of data bursts transmitted from the WTs to the BS (UC) and an uplink signalling phase (US). During US the WTs are able to send short signalling messages to the BS by using sub-slots, if they have no reserved slots to transmit them piggyback within a data burst. These signalling messages can be seen as dynamic parameters representing capacity requests of the WTs. For US a contention free and/or a contention based access scheme can be applied.

In the downlink phase a signalling burst (DS) and all data bursts from the BS to the WTs (DC) are transmitted. Inside DS are announcements of DC and US and reservations of UC for the current SP sent to the WTs. Additionally, DS contains feedback messages to earlier sent uplink signalling information (during US or piggyback within UC), which are e.g. necessary for collision resolution or functions such as automatic repeat request (ARQ) [4,8]. With this information the WTs exactly know when they are allowed to send or when they have to receive a burst.

III. PROCESSING DELAYS

In real W-ATM systems the above described MAC scheme has to be modified to handle the delays caused by the processing effort in the physical layer as well as in the DLC layer itself. These delays are defined in figure 2, which shows an example of a basic W-ATM system consisting of one BS and one WT. Both, BS and WT hold the following components:

- data link control (DLC) protocol unit
- base band processing unit (BBPU) including FEC
- millimetrewave transceiver (MWT)

Each of above elements adds a certain delay to data packets in transmit and receive direction. Especially generating of the downlink signalling information for DS and its decoding at the WTs turns out to be one key problem: After generation of the signalling data at the DLC layer in the BS it is sent to the physical layer and is processed in the baseband processing unit (BBPU), the FEC unit and the millimetrewave transceiver (MWT) before DS leaves the BS. At the WTs DS is received after the propagation delay of the transmission media and again processed in the physical and the DLC layer before the WTs are able to react on the received signalling information at the DLC layer.

The following table summaries the delays affecting the performance of MAC protocols:

Delay	Description
$t_{DLC,DS,Gen}$	generating of DS in DLC layer of BS
$t_{DLC,DS,Eval}$	evaluation of DS in DLC layer of WT
$t_{DLC,Send}$ $t_{DLC,Recv}$	sending/receiving of signalling or data burst at DLC layer of BS and WT
$t_{BBPU,Send}$ $t_{BBPU,Recv}$	baseband processing of signalling or data burst at BS and WT
$t_{FEC,Send}$ $t_{FEC,Recv}$	FEC processing of signalling or data at BS and WT
$t_{MWT,Send}$ $t_{MWT,Recv}$	MWT processing of signalling or data burst at BS and WT

For convenience it is assumed that BS and WT have equal delays. The resulting delay for the physical layer for sending and receiving a slot arises as follows:

$$t_{Phy,Send} = t_{FEC,Send} + t_{BBPU,Send} + t_{MWT,Send}$$
$$t_{Phy,Recv} = t_{FEC,Recv} + t_{BBPU,Recv} + t_{MWT,Recv}$$

Additionally, it has to be pointed out, that in these days implementations of W-ATM systems most of above delays are still in the order of one or more time slots of

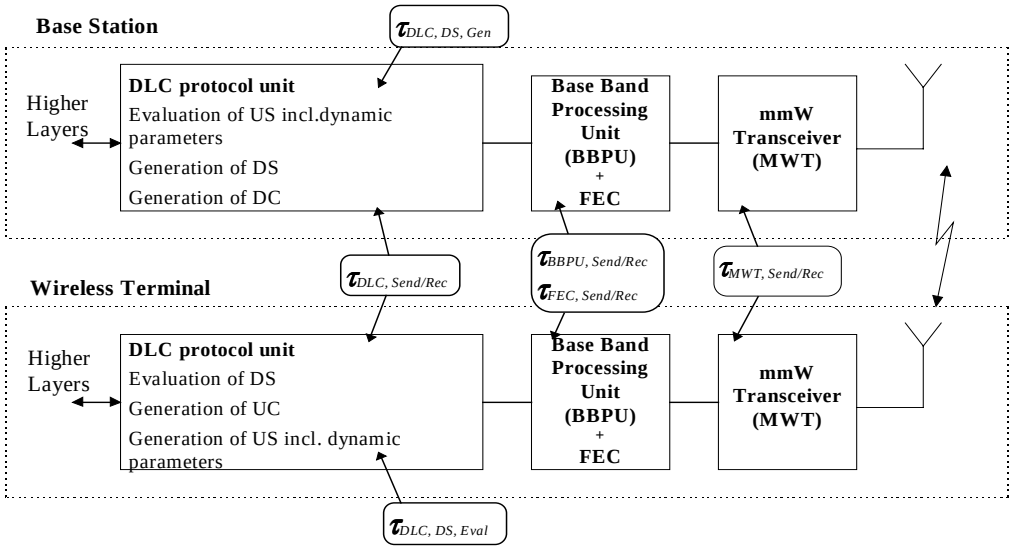

Figure 2 : Basic W-ATM system

the air interface. Especially generation of DS is time consuming. These facts have to be considered carefully to avoid unused capacity on the physical channel, which is important in case of high channel load.
Furthermore, the following rules have to be taken into account to increase dynamic behaviour and therefore performance of the protocol:

A) The DS should be generated as late as possible to consider the latest received information (independent whether this information was received via the air interface or the fixed ATM network).
B) Feedback from the previous uplink has to be processed at the BS and sent as early as possible to be considered by the WTs in the following uplink.
C) Signalling overhead has to be kept as low as possible.

Above properties lead to the definition of two parameters for a rough QoS estimate:

- Round trip delay (RTD) τ_{RTD} of the uplink signalling: The RTD is defined as the average delay between uplink signalling and the moment from which on it effects the further communication process. Basically, RTD is denoted by the feedback arrow from DS to US and UC (see figure 1).
- Signalling offset τ_{off} : The signalling offset is defined as the delay between the end of DS on the air interface and the start of the corresponding SP on the air.

IV. ENHANCED SIGNALLING

This section introduces an enhanced signalling scheme, taking delays and performance rules A) to C), presented in section III, into consideration. In contrast to the DSA++ protocol shown in figure 1, the enhanced signalling scheme divides up- and downlink phase UC and DC into several sub-phases as show in figure 3:

- $DC_{n,x}$: ATM cells of downlink sub-phase x in SP_n
- $UC_{n,x}$: ATM cells of uplink sub-phase x in SP_n

The general functionality of US and DS stays unchanged. That means DS_n consists of announcements for $DC_{n,x}$ and US_n and furthermore of reservations for $UC_{n,x}$. Additionally, DS_n contains feedback information for $UC_{n-1,\,1}$, US_{n-1}, $UC_{n-2,\,2}$ and $UC_{n-2,\,3}$. US_n is again used for uplink signalling via sub-slots (random access or polling) during SP_n.
The sub-phases allow flexible positioning of US_n and DS_{n+1} within SP_n to optimally adapt to the given processing delays. These delays lead to conditions for

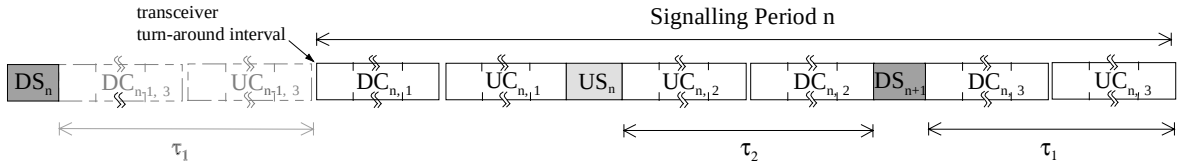

Figure 3: Enhanced signalling scheme

the sub-phases $UC_{n,2}/DC_{n,2}$ and $UC_{n,3}/DC_{n,3}$, which have to be considered by the MAC protocol.

First, the WTs must be able to evaluate and to react to the signalling information DS_n before the related SP_n starts. This has been denoted as required signalling offset t_{off} and leads to a relation for t_1:

$$t_1 \geq t_{off} = t_{Phy,Rec} + t_{DLC,Rec} + t_{DLC,DS,Eval} + t_{DLC,Send} + t_{Phy,Send}$$

Within the number of slots required to cover t_1, the ratio of $UC_{n,3}$ and $DC_{n,3}$ can be varied.

Second, the uplink signalling information arriving during generation of DS_{n+1} can not or only partly be considered for downlink signalling in DS_{n+1}. Additionally, DS_{n+1} should be based on the latest dynamic parameters sent by the WTs piggyback within data bursts $UC_{n,x}$ or during US_n. Because of the fact that in US_n sub-slots are used, the number of parameters per time interval is much higher compared to the piggyback transmission. Therefore, US_n should be considered for DS_{n+1}. This leads to a minimum signalling acceptance point of time (SAPT) t_{SAPT} for uplink signalling information, which can be defined relatively to the start of DS_{n+1} on the air interface and results in the following relation for t_2:

$$t_2 \geq t_{SAPT} = t_{Phy,Rec} + t_{DLC,Rec} + t_{DLC,DS,Gen} + t_{DLC,Send} + t_{Phy,Send}$$

Within the number of slots required to cover t_2, the ratio of $UC_{n,2}$ and $DC_{n,2}$ can be varied.

The MAC protocol has to choose the size of $DC_{n,x}$ and $UC_{n,x}$ in such a way that the time span of t_1 and t_2 can be covered by transmitting ATM cells, so that no capacity is lost. This is essential for high traffic load conditions. Also the number of TTIs inside one SP should be minimised. This suggests that the duration of $DC_{n,3}$ should fully cover t_1 and no additional uplink phase $UC_{n,3}$ is inserted.

Furthermore, flexibility demands that the MAC protocol can adapt to asymmetric load conditions caused by the scheduling algorithm or by the traffic type as e.g. distribution services like Video On Demand. These conditions are investigated in the following two examples.

Asymmetric Load: predominant downlink traffic

Even if there is no uplink traffic the WTs must have the opportunity to transmit their capacity requests or other signalling information to the BS. Therefore, an uplink signalling phase US_n is still required. The resulting signalling scheme can be derived from figure 3 by setting the duration of $UC_{x,n}$ to zero. Then the uplink phase only consists of uplink signalling US_n as shown in figure 4.

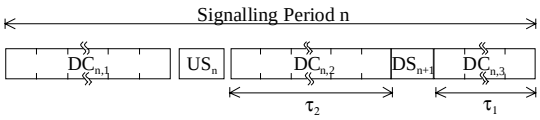

Figure 4: Predominant downlink traffic

Asymmetric Load: predominant uplink traffic

In case that SP_n only contains uplink cells, the duration of $DC_{n,x}$ in figure 3 can be set to zero. This results in the scheme presented in figure 5.

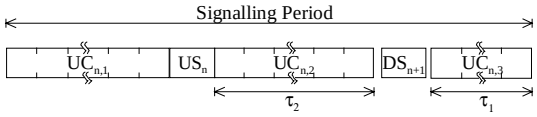

Figure 5: Predominant uplink traffic

Comparison with original DSA++ protocol considering processing delays

Besides the presented enhanced signalling scheme also some possible adaptations of the original DSA++ protocol to handle the given processing delays can be taken into consideration.

First, periods of no transmission can be inserted between US and DS, and DS and DC in figure 1 to cover the required processing time t_1 and t_2 This means, that nothing is transmitted during this time and capacity is lost. Obviously, this leads to waste of capacity and results in higher delays.

Second, DS can signal UC and US of SP and additionally DS and DC of the consecutive SP (see figure 1). Regarding the delay conditions for t_1 and t_2 it can be assumed that t_1 has to be met by DC while US can not be considered in the following DS, because of the delay condition for t_2. This means, the parameters which the capacity assignment is performed on are older than by using the enhanced signalling scheme. In other words, t_{RTD} is increased.

Both modifications of the original DSA++ reveal, that the enhanced signalling scheme is the more attractive solution. This statement will be proved by simulations in the following section.

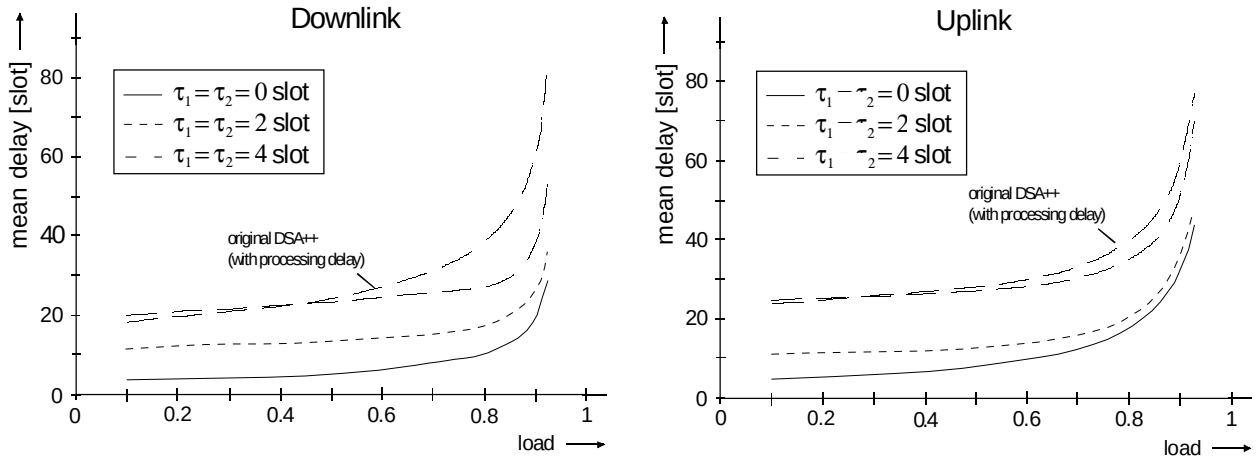

Figure 6: Mean transmission delay versus channel load

V. PERFORMANCE EVALUATION

In this section the performance of the enhanced signalling scheme is evaluated by simulation. In the first scenario the enhanced signalling scheme is examined by using Poisson Sources. In the second part of the evaluation a multimedia scenario is investigated. In both scenarios the enhanced signalling scheme is compared with the original DSA++ protocol without processing delays, describing the ideal case. Additionally, for a more realistic performance evaluation an adapted version of the DSA++ protocol, which is able to handle delays, is simulated (second example in section IV) and will be referred as *original DSA++ with processing delay*. For all simulations an error free channel is assumed, because only the behaviour of the MAC layer should be examined.

The following values are examined for the original DSA++ and the introduced enhanced signalling scheme for different processing delays:

- transmissions delay of ATM cells
- percentage of unused capacity to fulfil the requirements for t_1 and t_2 described above.
- number of transceiver-turn-around intervals (TTI).

The first simulation scenario consists of one BS serving 10 WTs. Each WT has established one bi-directional connection. The traffic sources were modelled with a Poisson Source and the load was distributed uniformly

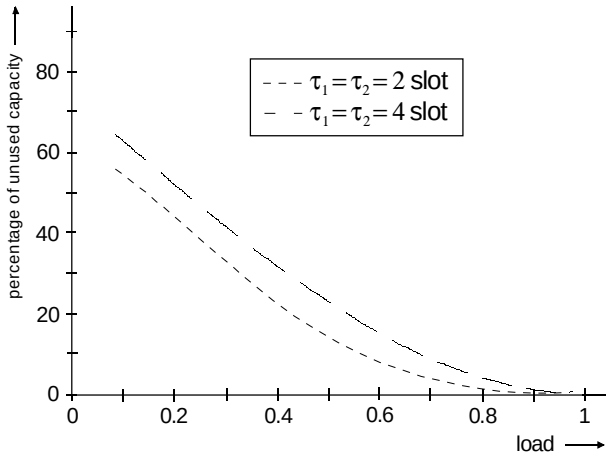

Figure 7: Percentage of unused capacityversus total channel load

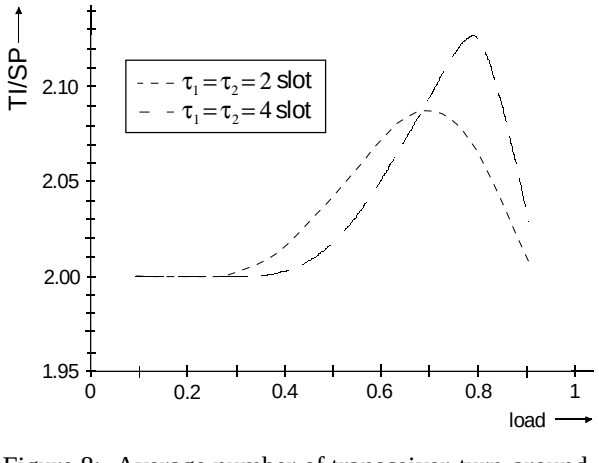

Figure 8: Average number of transceiver-turn-around intervals versus total channel load

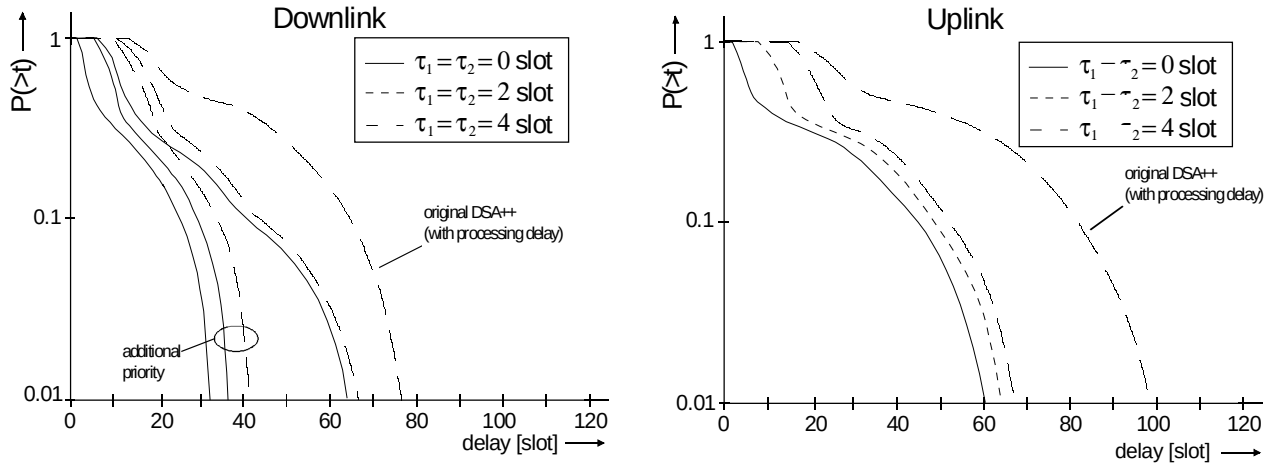

Figure 9: Complementary distribution function of the transmission delay for CBR services

between the WTs. The delay of the transmitted ATM cells as well as the processing delay have been normalised to the slot size of the air interface. The simulation were carried out for $t_1=t_2=2$ slots and $t_1=t_2=4$ slots for different overall loads.

Figure 6 shows the resulting mean transmission delay for up- and downlink traffic versus channel load. As expected, the transmission delay increases, if the processing delay increases due to two different aspects: First, the assignment of transmission capacity is based on dynamic parameters which are out of date. Second, capacity is lost because periods of no transmission are required to handle the processing delay. Also the resulting transmission delay of the original DSA++ protocol with processing delay in case of $t_1=t_2=4$ is shown in figure 6. It is visible that for low load (<30%) the original protocol is slightly better, while for higher load the enhanced signalling scheme leads to significantly smaller transmission delays.

The percentage of unused capacity is shown in figure 7. It can be seen that in case of relatively low load most of the transmission capacity is unused, since not enough ATM cells are available to cover the sub-phases UC_2/DC_2 and UC_3/DC_3. If the overall load is increased, the percentage of unused capacity is reduced.

Figure 8 shows the average number of TTIs per SP. During each SP at least two TTIs occur, since there is always an uplink and a downlink phase. Only if UC_3 is inserted (see figure 3), additional TTIs are required. Furthermore, it can be seen, that higher processing delay (higher values for t_1 and t_2) leads to less additional TTIs during medium load, because uplink slots can transmitted during the span of t_2 and the TTI between DC3 and UC3 can be avoided.

In the second simulation a multimedia scenario is chosen to evaluate the performance of the enhanced signalling scheme in a more realistic environment. The parameters of the scenario are as follows:

service	ATM class	λ p. VC	#WT	load	τ_{dmax}	τ_{dmax}/τ_{slots}
voice	CBR	64 Kbps	4	3%	3 ms	150
video	VBR	1.5Mbps	2	30%	20 ms	1000
data	ABR	1.6Mbps	2	32%	∞	∞

The scenario is evaluated for $t_1=t_2=2$ slots and $t_1=t_2=4$ slots.

Figure 9 shows the complementary distribution function (CDF) of the transmission delay for the CBR services. The processing time leads to a significant higher variance of the transmission delay, because in case of not enough downlink ATM cells the time critical cells of the CBR service are moved to the end of the signalling period (DC3). The variance of the transmission delay can be reduced, if time critical cells are moved from DC3 to DC1 (see figure 9: additional priority). If not enough slots are available, nothing is transmitted during t_2 and capacity is wasted. The resulting CDFs are also shown in figure 9. Since the total CBR traffic can be neglected, there is (nearly) no influence on the transmission delay of other services. For comparison the CDF of the original DSA++ protocol with processing delay is shown in case of $t_1=t_2=4$, which leads to higher delay. The evaluation of CBR traffic shows, that it is useful to implement special protocols for this kind of service class.

Regarding the CDFs of the VBR and ABR service, which are shown in figure 10 and 11, it can be seen, that the resulting delay is always less than in case of

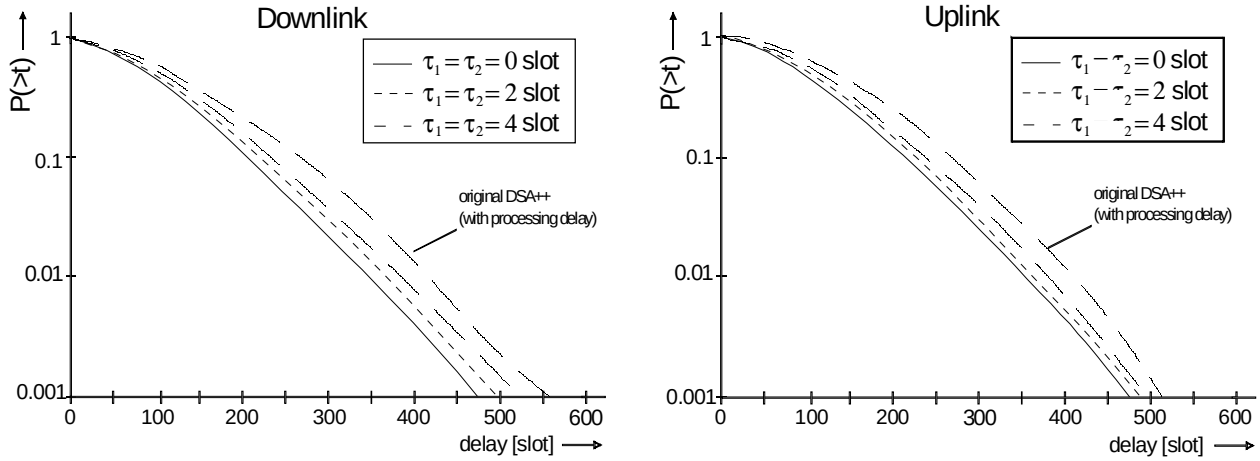

Figure 10: Complementary distribution function of the transmission delay for VBR services

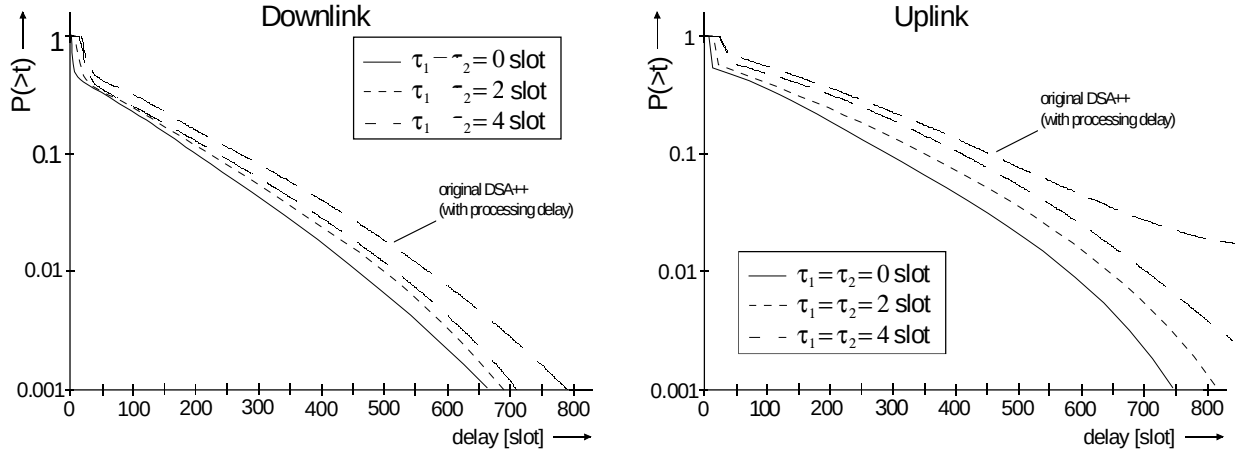

Figure 11: Complementary distribution function of the transmission delay for ABR services

the original DSA++ protocol with processing delays (t_1=t_2=4). Furthermore in figure 11 (especially uplink), which shows the CDF of ABR traffic, it can be seen that the introduced signalling scheme is able to carry higher traffic load.

VI. CONCLUSIONS

In real W-ATM systems processing delays in the physical layer and the DLC layer have to be taken into account by the MAC protocol. In general these delays lead to increased cell delay and CDV. With the proposed enhanced signalling scheme the effects of processing delays can significantly be reduced. This is achieved by dividing the SP in sub-phases, which can optimally be adapted to the processing delays and the current load situations.

The advantages of the new scheme were proved by detailed simulations where the enhanced signalling scheme has been examined and compared with the original DSA++ protocol (with processing delays).

Nevertheless, the principles of the enhanced signalling scheme were presented based on the DSA++ protocol, but they can also be used in most of the available MAC protocols for wireless ATM networks.

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